IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Mario I. Wolczko, Adam R. Talcott		
Assignee:	Sun Microsystems, Inc.		
Title:	Obtaining Execution Path Information in an Instruction Sampling System		
Serial No.:	10/784,730	Filing Date:	February 23, 2004
Examiner:	Brian P. Johnson	Group Art Unit:	2183
Docket No.:	SUN030248		

Austin, Texas
July 11, 2006

COMMISSIONER FOR PATENTS
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RESPONSE TO NON-FINAL OFFICE ACTION

Dear Sir:

This paper is responsive to the Office action dated April 19, 2006 having a shortened statutory period expiring July 19, 2006. Further examination and reconsideration are respectfully requested in view of the amendments and remarks set forth below.

AMENDMENTS

To the Title

Please replace the title with the following new title:

OBTAINING EXECUTION PATH INFORMATION IN AN INSTRUCTION SAMPLING SYSTEM BY LINKING CONTROL TRANSFER INFORMATION WITH SAMPLING INFORMATION

In the Claims

1. (Currently Amended) A method of linking control transfer information with sampling information for instructions executing in a processor comprising:

storing information relating to execution events in a history queue;

selecting an instruction for sampling;

storing information relating to the instruction for sampling;

freezing the information relating to execution events in the history queue when the information relating to the instruction for sampling is to be reported to provide frozen execution event information;

reporting the information relating to the instruction for sampling; and,

enabling access to the frozen execution event information in the history queue.

2. (Original) The method of claim 1 further comprising:

freezing the execution event information provides information to enable reconstructing an execution path of events adjoining the instruction.

3. (Original) The method of claim 1 wherein:

the storing information relating to execution events and the storing information relating to the instruction occur within separate structures of a processor.

4. (Original) The method of claim 1 wherein:

the freezing the information relating to execution events disables storing of additional information relating to execution events.

5. (Original) The method of claim 1 further comprising:

enabling storing information relating to execution events occurring after execution of the instruction for sampling.

6. (Currently Amended) An apparatus for linking control transfer information with sampling information for instructions executing in a processor comprising:

means for storing information relating to execution events in a history queue;

means for selecting an instruction for sampling;

means for storing information relating to the instruction;

means for freezing the information relating to execution events in the history queue when the information relating to the instruction for sampling is to be reported to provide frozen execution event information;

means for reporting the information relating to the instruction; and,

means for enabling access to the frozen execution event information in the history queue.

7. (Original) The apparatus of claim 6 wherein:

means for freezing the execution event information provides information to enable reconstructing an execution path of events adjoining the instruction.

8. (Original) The apparatus of claim 6 wherein:

the means for storing information relating to execution events and the means for storing information relating to the instruction are located within separate modules of a processor.

9. (Original) The apparatus of claim 6 wherein:

the freezing the information relating to execution events disables storing of additional information relating to execution events.

10. (Original) The apparatus of claim 6 further comprising:

means for enabling storing information relating to execution events occurring after execution of the instruction for sampling.

11. (Original) A processor comprising:

an instruction pipeline;

a sampling mechanism coupled to the instruction pipeline, the sampling mechanism selecting an instruction for sampling and storing information relating to the instruction for sampling;

a history queue coupled to the pipeline, the history queue storing information relating to execution events, the history queue freezing the information relating to execution events when the information relating to the instruction for sampling is to be reported to provide frozen execution event information so as to enable linking control transfer information with sampling information for instructions executing in the processor.

12. (Original) The processor of claim 11 wherein:
the sampling mechanism reports the information relating to the instruction for sampling.

13. (Original) The processor of claim 11 wherein:
the history queue enables access to the frozen execution event information.

14. (Original) The processor of claim 11 wherein:
freezing the execution event information provides information to enable reconstructing an execution path of events adjoining the instruction.

15. (Original) The processor of claim 11 wherein:
freezing the information relating to execution events disables storing of additional information relating to execution events.

16. (Original) The processor of claim 11 wherein:
the history queue stores information relating to execution events occurring after execution of the instruction for sampling.

17. (Currently Amended) A method of monitoring control transfer information for instructions executing in a processor comprising:
storing information relating to execution events in a history queue;
freezing the information relating to execution events in the history queue when the information relating to the instruction is to be reported to provide frozen execution event information; and,
enabling access to the frozen execution event information in the history queue.

18. (Original) The method of claim 17 wherein:

the freezing occurs based upon an instruction sample being reported.

REMARKS

Claims 1 - 18 are pending in the application. Claims 1- 18 have been rejected. Claims 1, 6 and 17 have been amended. No new claims have been added.

Claims 1 - 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chrysos, U.S. Patent No. 6,148,396 (Chrysos).

The present invention generally relates to coupling a sampling mechanism and a history queue to allow reconstruction of a path leading up to a sample. The history queue enables a processor to provide information which software can then use to reconstruct the flow of execution through an instruction space. (See e.g., Wolczko Application, page 5, lines 17 – 22.)

More specifically, the present invention, as set forth by independent claim 1, relates to a method of linking control transfer information with sampling information for instructions executing in a processor. The method includes storing information relating to execution events in a history queue, selecting an instruction for sampling, storing information relating to the instruction for sampling, freezing the information relating to execution events in the history queue when the information relating to the instruction for sampling is to be reported to provide frozen execution event information, reporting the information relating to the instruction for sampling, and enabling access to the frozen execution event information in the history queue.

The present invention, as set forth by independent claim 6, relates to an apparatus for linking control transfer information with sampling information for instructions executing in a processor. The apparatus which includes means for storing information relating to execution events in a history queue, means for selecting an instruction for sampling, means for storing information relating to the instruction, means for freezing the information relating to execution events in the history queue when the information relating to the instruction for sampling is to be reported to provide frozen execution event information, means for reporting the information relating to the instruction, and means for enabling access to the frozen execution event information in the history queue.

The present invention, as set forth by independent claim 11, relates to a processor which includes an instruction pipeline, a sampling mechanism coupled to the instruction pipeline and a history queue coupled to the pipeline. The sampling mechanism selects an instruction for sampling and storing information relating to the instruction for sampling. The history queue stores information relating to execution events and freezes the information relating to execution events when the information relating to the instruction for sampling is to be reported to provide frozen execution event information so as to enable linking control transfer information with sampling information for instructions executing in the processor.

The present invention, as set forth by independent claim 17, relates to a method of monitoring control transfer information for instructions executing in a processor. The method includes storing information relating to execution events in a history queue, freezing the information relating to execution events in the history queue when the information relating to the instruction is to be reported to provide frozen execution event information, and enabling access to the frozen execution event information in the history queue.

Chrysos relates to sampling path history information of executing instructions. Chrysos discloses an apparatus for collecting state information associated with an execution path of recently processed instructions in a processor pipeline of a computer system. The apparatus identifies a class of instructions to be sampled. Path-identifying state information of a currently processed instruction is sampled when the currently processed instruction belongs to the identified class of instructions.

Chrysos sets forth

> Periodically, during operation of a processor, an instruction to be profiled is randomly selected, and a profile record of what happens during the execution of the instruction is accumulated in a set of internal profile registers of the processor. After processing ***of the selected instruction*** terminates, e.g., the instruction retires, aborts or traps, an interrupt is generated. The recorded information characterizing the details of how the instruction was processed in the pipeline can be sampled from the internal profile registers by software.
>
> The profile registers can record many useful facts about an instruction's execution. Example, performance information can include: the number of cycles the selected instruction spent in each state of an execution pipeline, i.e., stage latencies, whether the instruction suffered I-cache or D-cache misses, the effective addresses of its

memory operands, or ***branch/jump targets***, and whether the instruction was retired or aborted. (Chrysos, Col. 5, lines 44 – 61, emphasis added.)

Accordingly, Chrysos discloses accumulating the profile during the execution of the instruction and reporting this profile information after processing of the instruction terminates. While Chrysos discloses as an example of performance information branch or jump targets of the instruction, there is no disclosure in Chrysos of maintaining a history queue in which execution events are stored. The memory for storing profile information for each instruction being sampled of Chrysos (see e.g., Chrysos Fig. 3 and Col. 11, lines 30 – 36) merely stores information for the instruction being sampled, not for instruction events which would enable an instruction flow to be reconstructed as is possible by linking a history queue with a sampling mechanism in the present invention.

More specifically, Chrysos does not teach or suggest a method of *linking control transfer information with sampling information* for instructions executing in a processor, much less such a method which includes *storing information relating to execution events in a history queue*, *freezing the information relating to execution events in the history queue when the information relating to the instruction for sampling is to be reported to provide frozen execution event information*, or *enabling access to the frozen execution event information in the history queue*, all as required by claim 1. Accordingly, claim 1 is allowable over Chrysos. Claims 2 - 5 depend from claim 1 and are allowable for at least this reason.

Chrysos does not teach or suggest an apparatus for *linking control transfer information with sampling information* for instructions executing in a processor, much less such an apparatus which includes means for *storing information relating to execution events in a history queue*, means for *freezing the information relating to execution events in the history queue when the information relating to the instruction for sampling is to be reported to provide frozen execution event information*, or *means for enabling access to the frozen execution event information in the history queue*, all as required by claim 6. Accordingly, claim 6 is allowable over Chrysos. Claims 7 - 10 depend from claim 6 and are allowable for at least this reason.

Chrysos does not teach or suggest a processor which includes an instruction pipeline, a sampling mechanism coupled to the instruction pipeline and *a history queue* coupled to the

pipeline, much less such a processor where the history queue *stores information relating to execution events and freezes the information relating to execution events when the information relating to the instruction for sampling is to be reported to provide frozen execution event information so as to enable linking control transfer information with sampling information for instructions executing in the processor*, all as required by claim 11. Accordingly, claim 11 is allowable over Chrysos. Claims 12 - 16 depend from claim 11 and are allowable for at least this reason.

Chrysos does not teach or suggest a method of monitoring control transfer information for instructions executing in a processor which includes *storing information relating to execution events in a history queue, freezing the information relating to execution events in the history queue when the information relating to the instruction is to be reported to provide frozen execution event information in the history queue*, and *enabling access to the frozen execution event information*., all as required by claim 17. Accordingly, claim 17 is allowable over Chrysos. Claim 18 depends from claim 17 and is allowable for at least this reason.

CONCLUSION

The Specification has been amended to improve clarity. In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

The Commissioner is authorized to deduct any additional fees which may be necessary and to credit any overpayment to Deposit Account No. 502264.

I hereby certify that this correspondence is being electronically submitted to the COMMISSIONER FOR PATENTS via EFS on July 11, 2006.

/Stephen A. Terrile/

Attorney for Applicant(s)

Respectfully submitted,

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